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**APPLICANTS: Morgan Paul; Flynn Patrick; Fucsko Janos; + 689						
**CONTINUING DATA VERIFIED: LAK none 6/10/03 LAK none 11/20/03						
**FOREIGN APPLICATIONS VERIFIED: LAK none 6/10/03 LAK none 11/20/03						
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Foreign priority claimed <input type="checkbox"/>		35 USC 119 conditions met <input type="checkbox"/>		Verified and Acknowledged Examiners' initials <i>[Signature]</i>		
TITLE : Etching processes for integrated circuit manufacturing including methods of forming capacitors <small>U.S. DEPT. OF COM. / PAT. & TM. / PTO-435, (Rev. 12-94)</small>						

Primary Examiner [Signature] DISCLOSED	PREPARED FOR REVIEW [Signature] WARNING: The information disclosed here is confidential. Unauthorized disclosure may be prohibited by the Espionage Laws, Sections 122, 181 and 364, Penalties include the U.S. Federal Penalties. Office is restricted to authorized employees and contractors only.
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